IN THE CLAIMS:

The following is a current listing of claims and will replace all prior versions and listings of claims in the application. Please amend the claims as follows:

Claims 1-133 (Cancelled).

134. (Currently Amended) A semiconductor device, comprising:

a memory transistor having a composite gate structure containing a first conductive film, a first insulating film, and a second conductive film that overlie a first channel region, wherein said first conductive film is disposed closer to said first channel region than said second conductive film; and

a peripheral transistor having a single gate structure containing a third conductive film and a fourth conductive film that overlie a second channel region and are in contact over their cross-sections, wherein said third conductive film is disposed closer to said second channel region than said fourth conductive film;

~~wherein said first conductive film and said third conductive film are fabricated from a first common polysilicon layer, and wherein an impurity concentration of said first conductive film and an impurity concentration of said third conductive film are independent of one another~~

wherein said second, third, and fourth conductive films each have a conductivity that is substantially the same and that is higher than a conductivity of said first conductive film.

135. (Cancelled).

136. (Currently Amended) The semiconductor device of claim [[135]]134, wherein said first conductive film and said third conductive film have substantially the same thickness.

137. (Previously Presented) The semiconductor device of claim 136, wherein said second conductive film and said fourth conductive film have substantially the same thickness.

138. (Currently Amended) The semiconductor device of claim 137, wherein said second conductive film, said third conductive film, and said fourth conductive film have ~~substantially the same~~ an impurity concentration that is substantially the same and that is at least 10 times an impurity concentration of said first conductive film.

139-141. (Cancelled).

142. (Currently Amended) The semiconductor device of claim [[140]]134, wherein ~~said~~ an impurity concentration of said first conductive film is between $1x10^{18}$ and $1x10^{19}$ atoms/cm^3.

143. (Currently Amended) The semiconductor device of claim 142, wherein ~~said~~ an impurity concentration of said third conductive film is between $1x10^{20}$ and $1x10^{21}$ atoms/cm^3.

144. (Currently Amended) The semiconductor device of claim 143, wherein ~~said~~ an impurity concentration of said second conductive film is between $1x10^{20}$ and $1x10^{21}$ atoms/cm^3.

145. (Currently Amended) The semiconductor device of claim 144, wherein ~~said~~ an impurity concentration of said fourth conductive film is between $1x10^{20}$ and $1x10^{21}$ atoms/cm^3.

146-151. (Cancelled).

152. (New) The semiconductor device of claim 134, wherein said first, second, third, and fourth conductive films are polycrystalline silicon films.

153. (New) The semiconductor device of claim 134, wherein said first insulating film is a silicon oxide/silicon nitride/silicon oxide (ONO) film.

154. (New) The semiconductor device of claim 134, wherein said first conductive film is doped with phosphorous.

155. (New) The semiconductor device of claim 134, wherein said first conductive film is doped with arsenic.

156. (New) The semiconductor device of claim 134, wherein the semiconductor device is an EEPROM.

157. (New) The semiconductor device of claim 134, wherein the semiconductor device is an EPROM.

158. (New) The semiconductor device of claim 134, wherein said second, third, and fourth conductive films have substantially the same resistance.

159. (New) A method of manufacturing a semiconductor device having a first region and a second region, the method comprising:

forming a first oxide film over a substrate in said first region;

forming a second oxide film in said second region;

disposing a first conductive layer over said substrate, said first oxide film, and said second oxide film;

introducing impurities into said first conductive layer;

disposing a first insulating layer over said first conductive layer;

removing said first insulating layer over said second region;

disposing a second conductive layer over said first insulating layer and said first conductive layer such that said first and second conductive layers are separated by said first insulating layer in said first region and are in contact with each other over their cross-sections in said second region;

introducing impurities into said second conductive layer such that said second conductive layer has a conductivity that is higher than said first conductive layer in said first region, and such that first and second conductive layers have substantially the same conductivity in said second region.

160. (New) The method of claim 159, further comprising patterning said first region to form a memory cell transistor and patterning said second region to form a peripheral transistor.

161. (New) The method of claim 159, wherein said forming said first oxide film includes forming a tunnel oxide film by thermal oxidation.

162. (New) The method of claim 159, further comprising forming said second oxide film over a third oxide film in said second region.

163. (New) The method of claim 162, wherein said third oxide film is a field oxide film formed by the LOCOS method.

164. (New) The method of claim 162, wherein said second oxide film is a gate oxide film formed by thermal oxidation.

165. (New) The method of claim 159, wherein said impurities introduced into said first conductive layer are phosphorous impurities.

166. (New) The method of claim 159, wherein said impurities introduced into said first conductive layer are arsenic impurities.

167. (New) The method of claim 159, wherein said introducing impurities into said first conductive layer is by ion injection.

168. (New) The method of claim 159, wherein said introducing impurities into said second conductive layer is by vapor phase diffusion.

169. (New) The method of claim 159, wherein said introducing impurities into said first conductive layer and said introducing impurities into said second conductive layer is performed such that second conductive layer has an impurity concentration at least 10 times that of said first conductive layer in said first region.

170. (New) A semiconductor device, comprising:

a memory transistor having a composite gate structure containing a first conductive film, a first insulating film, and a second conductive film that overlie a substrate, wherein said first conductive film is separated from said substrate by a tunnel oxide layer, and wherein said first conductive film is separated from said second conductive film by said first insulating film; and

a peripheral transistor having a single gate structure containing a third conductive film and a third conductive film that overlie said substrate, wherein said fourth conductive film is on top of said third conductive film, and wherein said third and fourth conductive films are in

contact over their cross-sections;

wherein said second, third, and fourth conductive films each have a conductivity that is substantially the same and that is higher than a conductivity of said first conductive film.

171. The semiconductor device of claim 170, wherein a gate oxide film and a field oxide film are between said substrate and said third conductive film.

172. The semiconductor device of claim 170, wherein said second conductive film, said third conductive film, and said fourth conductive film have an impurity concentration that is substantially the same and that is at least 10 times an impurity concentration of said first conductive film.